INTEGRATED CIRCUITS

DATA SHEET

TDA7040T

Low voltage PLL stereo decoder

Product specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Low voltage PLL stereo decoder TDA7040T

GENERAL DESCRIPTION

The TDA7040T is a monolithic integrated circuit for low cost FM stereo radios with an absolute minimum of peripheral components and a simple lay-out.

Features

- Built-in four pole low pass filter with a 70 kHz corner frequency suppressing unwanted out-of-band input signals
- Fully integrated 228 kHz oscillator
- Pilot presence detector and soft mono/stereo blend
- Built-in interference suppression
- External stereo lamp driver applicable
- Adjustable gain.

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current V_P = 3 V	I_P	–	3	–	mA
Total harmonic distortion	THD	–	0,3	–	%
Signal to noise ratio	S/(S + N)	–	70	–	dB
Channel separation	α	–	40	–	dB

PACKAGE OUTLINE

8-lead mini-pack; plastic (S08; SOT96A); SOT96-1; 1996 July 24.

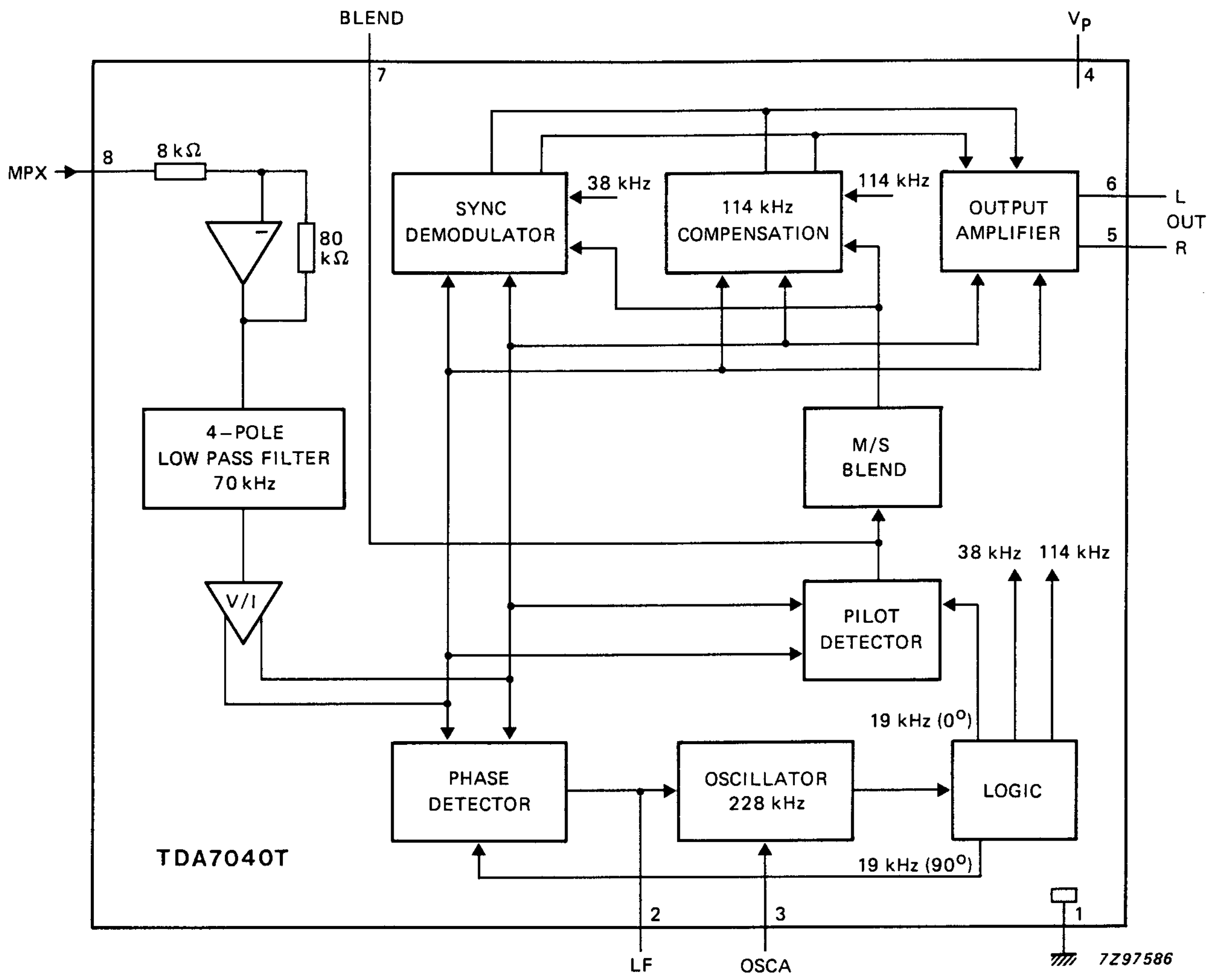


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range	V_P	–	–	7	V
Operating ambient temperature	T_{amb}	–10	–	+ 70	°C
Storage temperature range	T_{stg}	–55	–	+ 150	°C

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; test circuit Fig.2; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V_P	1,8	3,0	6,0	V
Supply current	I_P	–	3	4	mA
Output voltage (r.m.s. value)					
$V_{i(rms)}$ L and R 120 mV;					
f = 1 kHz	$V_{5,\,6\text{-}1}$	–	240	–	mV
Channel balance					
$V_{i(rms)}$ L and R 40mV;					
f = 1 kHz	ΔG_v	–	0	1	dB
Output resistance	R_O	–	5	–	kΩ
Total harmonic distortion					
$V_{i(rms)}$ L and R 40 mV;					
f = 1 kHz	THD	–	0,1	–	%
Total harmonic distortion					
$V_{i(rms)}$ L and R 40 mV;					
f = 1 kHz; $V_{p(rms)}$ = 12 mV	THD	–	0,3	–	%
Signal-to-noise ratio					
$V_{i(rms)}$ = 120 mV; f = 1 kHz	S/(S + N)	–	70	–	dB
Signal-to-noise ratio					
$V_{i(rms)}$ = 120 mV; f = 1 kHz					
$V_{p(rms)}$ = 12 mV	S/(S + N)	–	70	–	dB
Channel separation					
$V_{i(rms)}$ L and R 40 mV;					
f = 1 kHz; $V_{p(rms)}$ = 12 mV	α	–	40	–	dB
Capture range					
$V_{p(rms)}$ = 12 mV; deviation from					
centre frequency	Δf	–	± 3	–	%
Carrier leak					
$V_{i(rms)}$ L and R 120 mV;					
$V_{p(rms)}$ = 12 mV; f = 1 kHz;					
f = 19 kHz		–	30	–	dB
f = 38 kHz		–	50	–	dB
SCA (Subsidiary Communications					
Authorization) rejection					
$V_{i(rms)}$ L and R 120 mV;					
$V_{p(rms)}$ = 12 mV; f = 1 kHz;					
$V_{SCA(RMS)}$ = 12 mV; f = 67 kHz	α_{67}	–	70	–	dB

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ACI (Adjacent channel interference)					
$V_{i(rms)}$ L and R 120 mV;					
$V_{p(rms)}$ = 12 mV; f = 1 kHz;					
$V_{ACI(RMS)}$ = 1,3 mV; f = 114 kHz	α_{114}	–	90	–	dB
$V_{ACI(RMS)}$ = 1,3 mV; f = 190 kHz	α_{119}	–	85	–	dB
Traffic radio (V.W.F.) suppression	$\alpha_{57(VWF)}$	–	75	–	dB
$\alpha_{57\,(VWF)} = \frac{V_{o\,(signal)}\ (\text{at 1 kHz})}{V_{o\,(spurious)}\ (\text{at 1 kHz} \pm 23\ \text{Hz})}$					
measured with: 91% stereo signal; f_m = 1 kHz;					
9% pilot signal; 5% traffic subcarrier					
(f = 57 kHz, f_m = 23 Hz AM, m = 60%)					

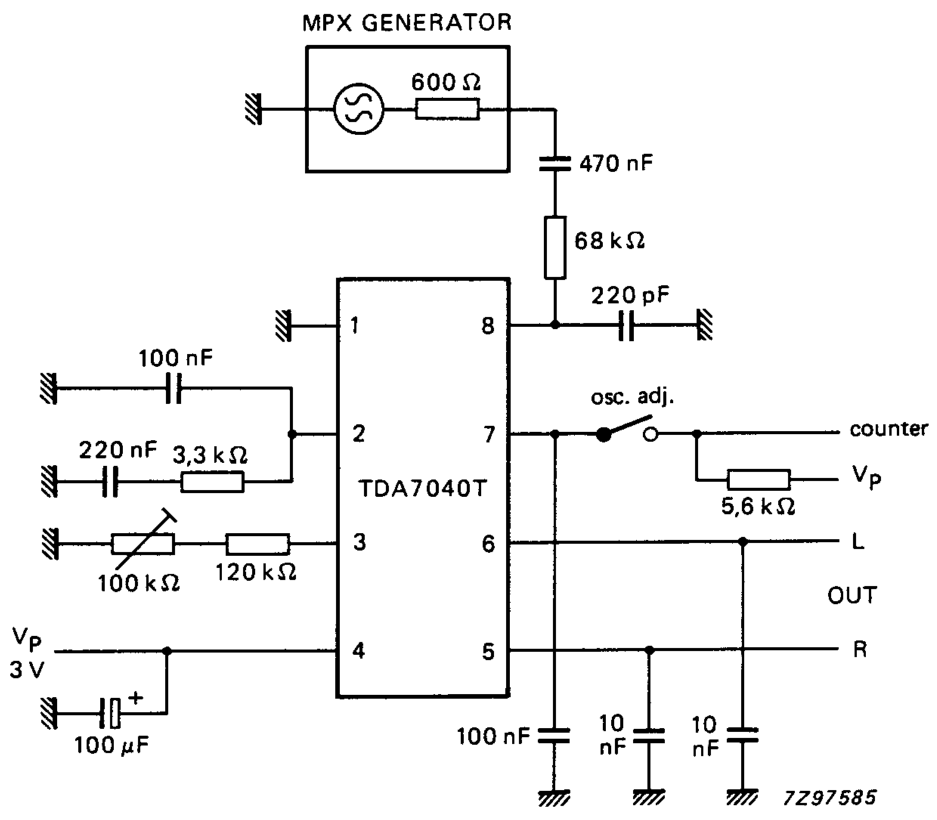


Fig.2 Test circuit.

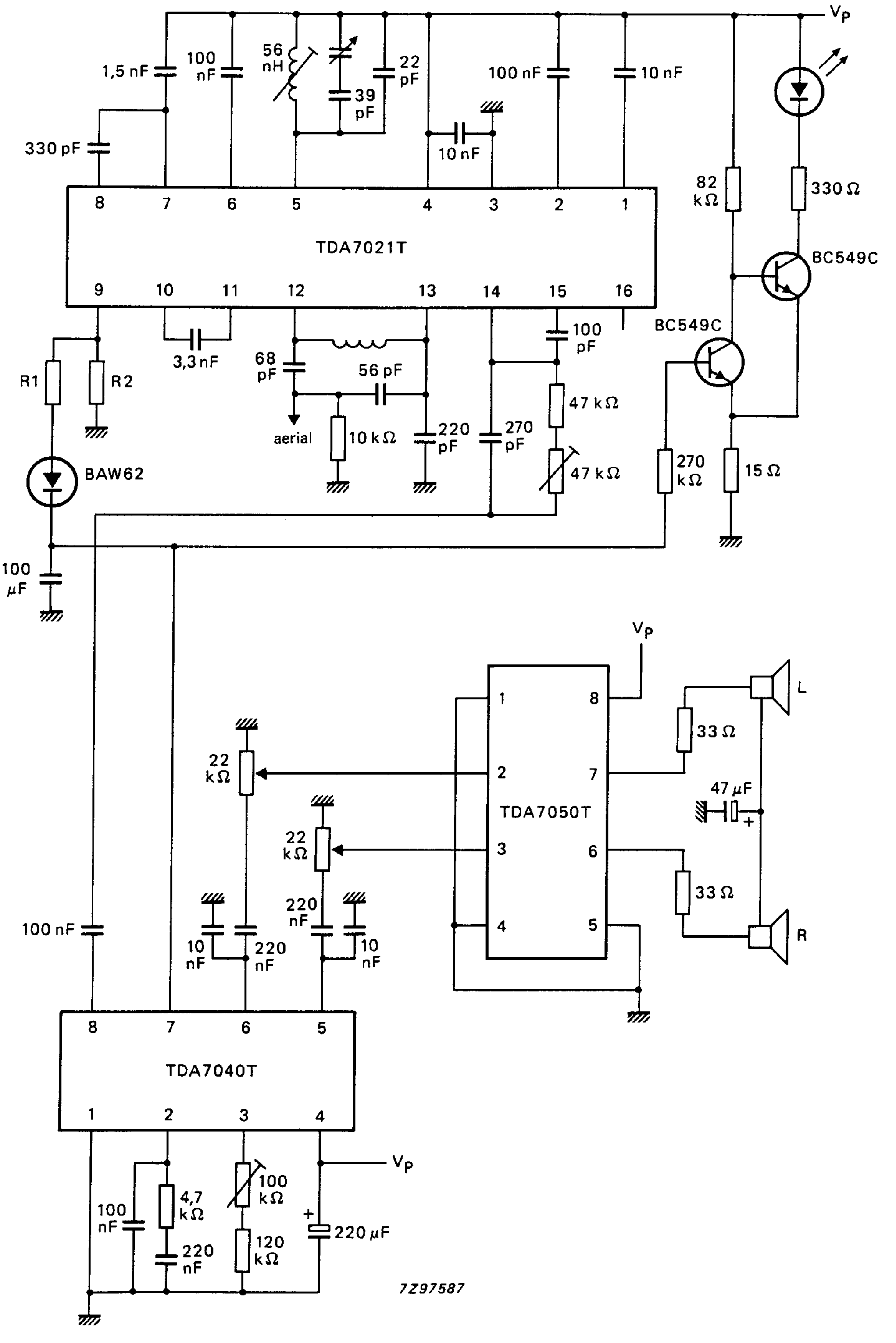


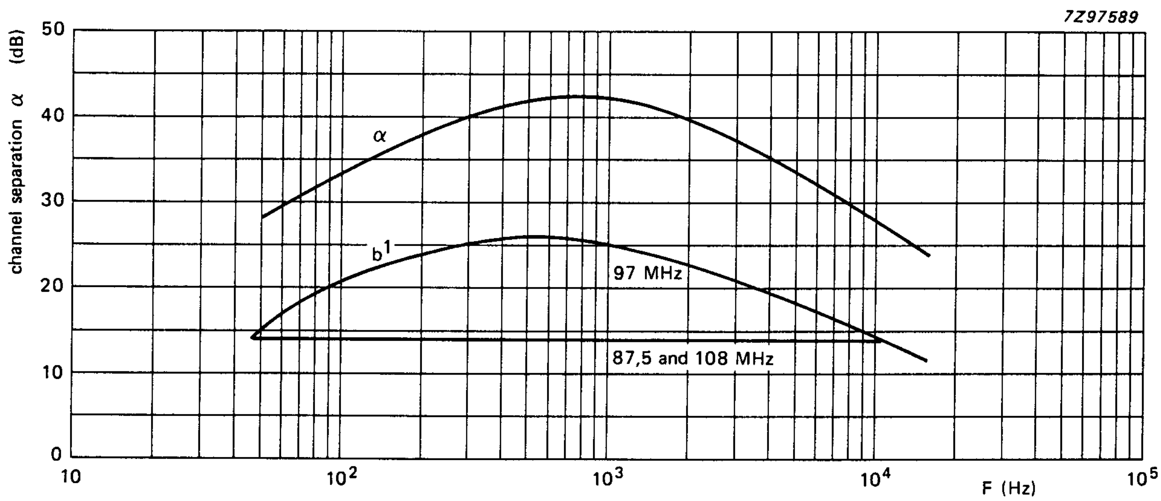
Fig.3 Application diagram in combination with TDA7021T and TDA7050T.

CHARACTERISTICS

Of the combination TDA7021T, TDA7040T and TDA7050T (Fig.3).

Conditions unless otherwise specified: $V_{vhf(rms)}$ = 1 mV; f_{hf} = 97 MHz; f_{dev} = 22,5 kHz; $f_{dev\ pilot}$ = 6,75 kHz; noise measured unweighted in a range from 400 Hz to 15 kHz.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Total harmonic distortion (pilot on)					
V_i = (L + R) signal; f_{mod} = 1 kHz	THD	–	0,5	–	%
V_i = L signal; f_{mod} = 1 kHz	THD	–	1,0	–	%
Signal to noise ratio					
V_i = (L + R) signal; f_{mod} = 1 kHz					
pilot off	S/(S + N)	–	56	–	dB
pilot on	S/(S + N)	–	50	–	dB
Channel separation					
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 97 MHz	α	–	26	–	dB
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 87,5 MHz and 108 MHz	α	–	14	–	dB
Output voltage (pilot off)					
V_i = (L + R) signal, f_{mod} = 1 kHz	$V_{o(rms)}$	–	80	–	mV



a = measured in test circuit (Fig.2)
b = measured in application diagram (Fig.3)

Fig.4 Channel separation as a function of audio frequency.

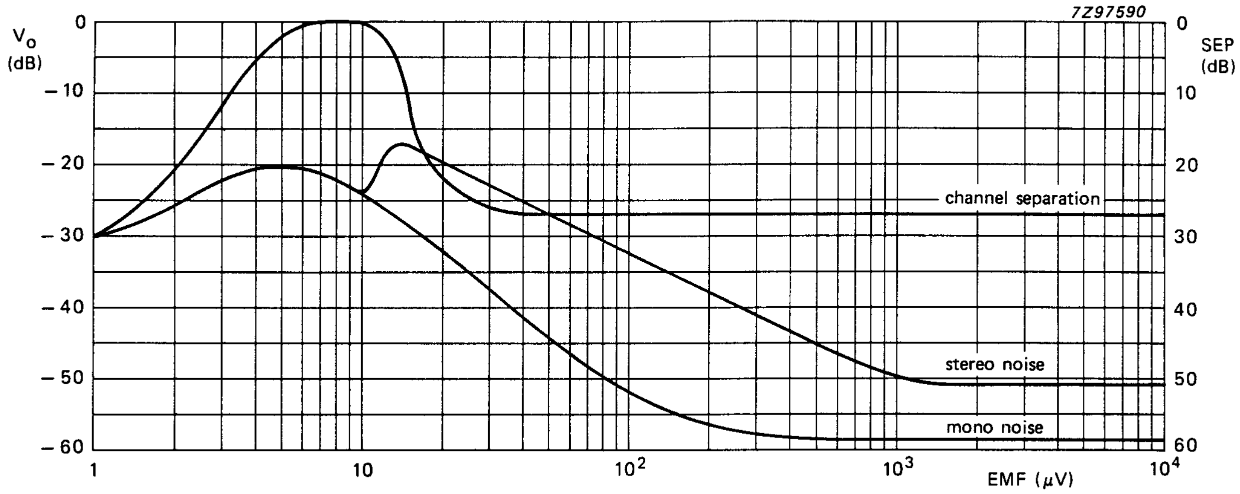


Fig.5 Signal/noise and channel separation behaviour in Fig.3. at R1 = 270 kΩ and R2 = 13 kΩ; without diode BAW62.

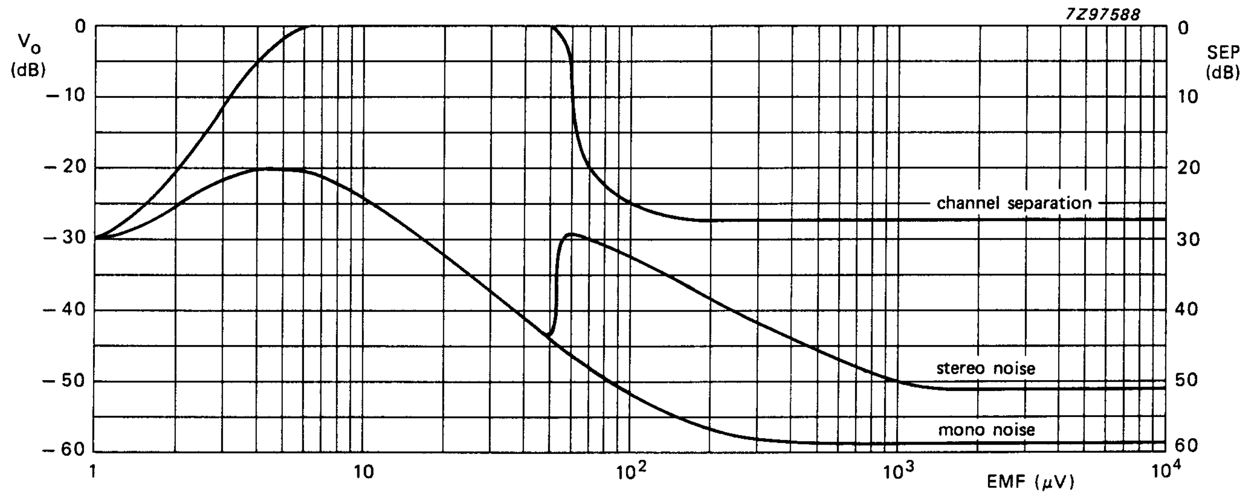
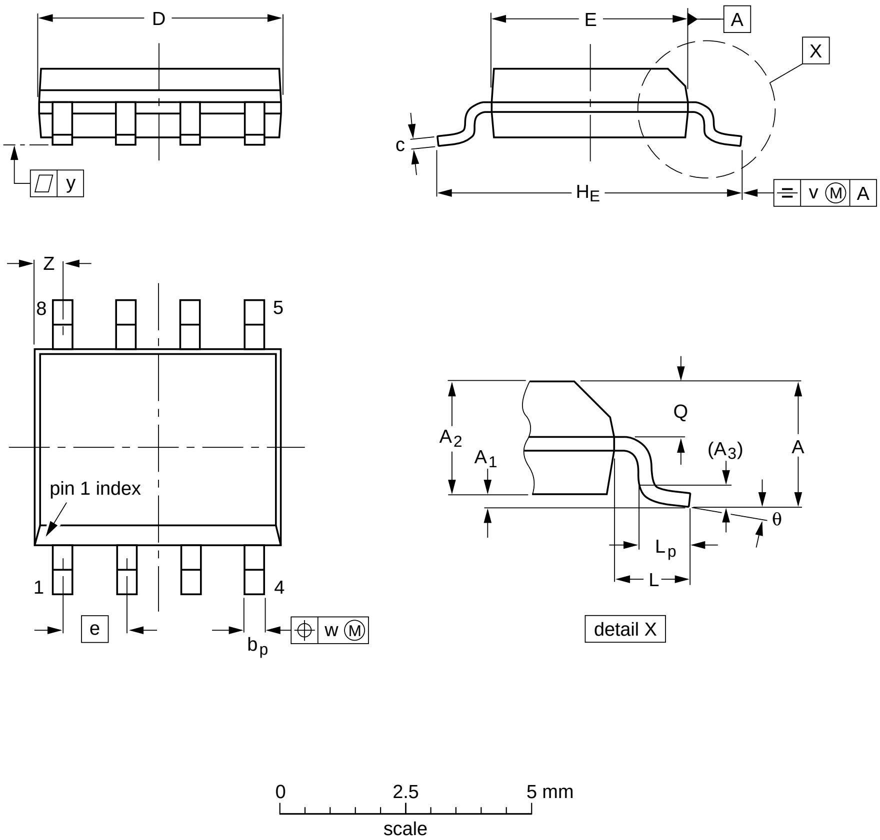


Fig.6 Signal/noise and channel separation behaviour in Fig.3. at R1 = 200 kΩ, R2 = 30 kΩ; with diode BAW62.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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